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performance • Stalls
impede progress of a
pipeline and result in
deviation from 1
instruction
executing/clock cycle •
CPI pipelined = - Ideal
CPI + Pipeline stall

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cycles per instruction -

$1 + \text{Pipeline stall cycles per instruction}$ •

Ignoring overhead and assuming stages are balanced: • Ideally, speedup equal to # of

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1.1 Computer architecture. refers to those attributes of a system visible to a programmer or, put another way, those attributes that have a direct impact on the logical execution of a program. Computer organization. refers to the operational units and their interconnections that realize the architectural specifications.

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computer, programs
are represented in a
form suitable for
storing in memory
alongside the data.

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